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- IEEE與IEEE Xplore簡介
- 高效檢索科研論文
- 搜索追蹤學術熱點
- 文獻綜述淺談

the Institute of Electrical and Electronics Engineers

電氣電子工程師學會

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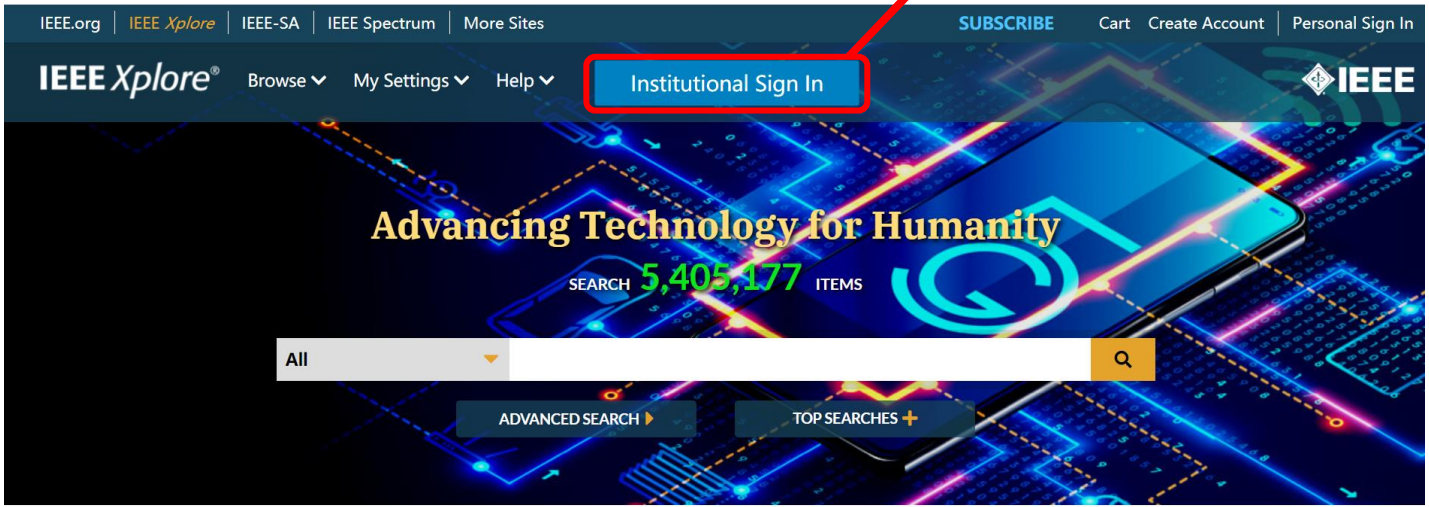

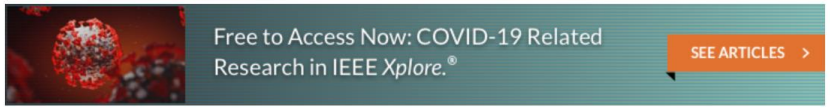

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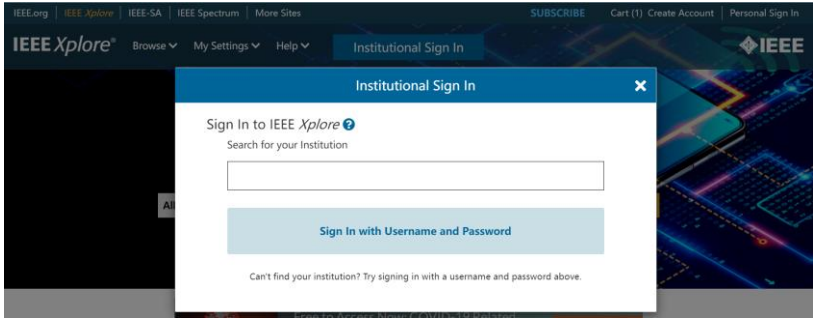

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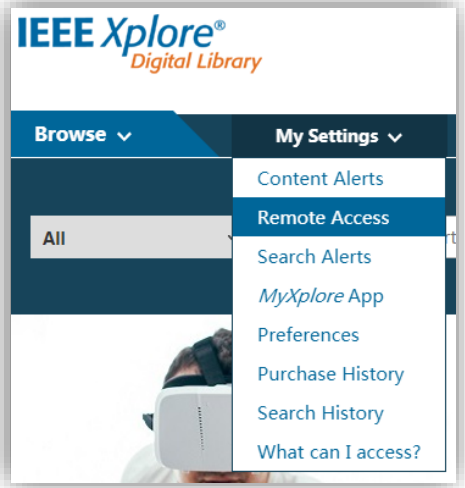

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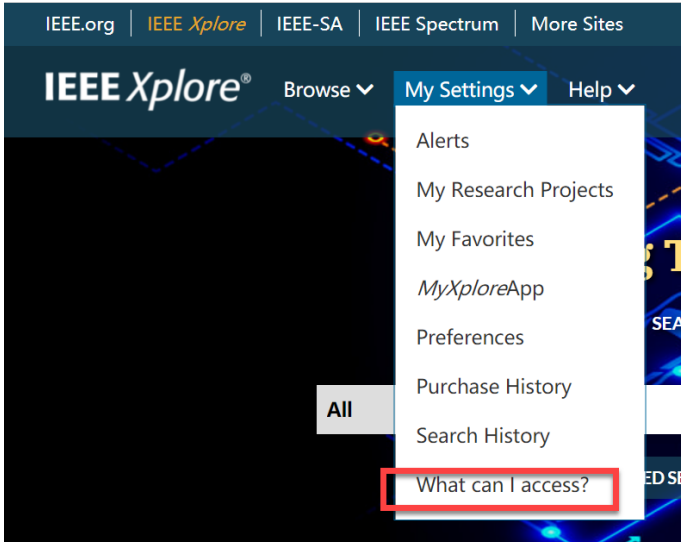

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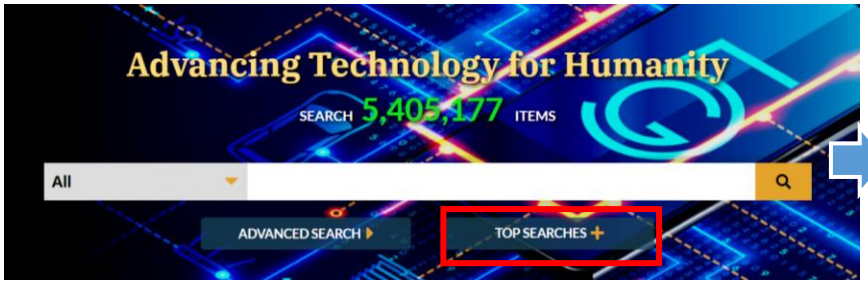

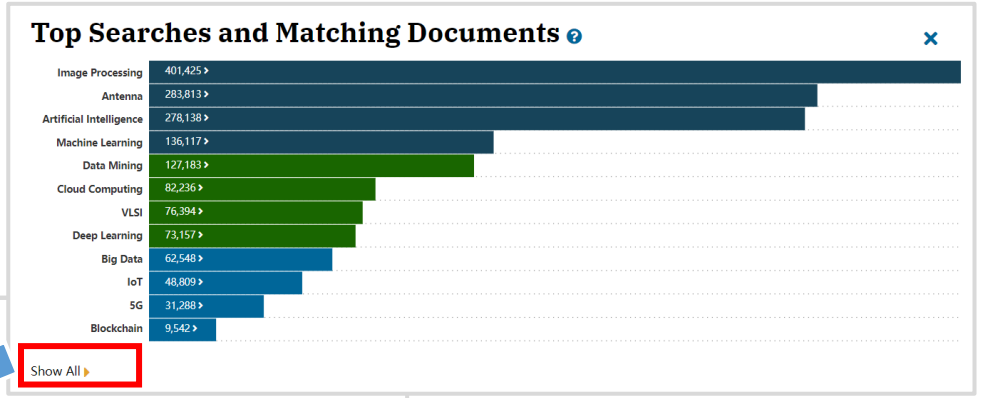

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Proceedings of the IEEE
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Biography
Raymond W. Yeung (Fellow, IEEE) was born in Hong Kong in June 1962. He received the B.S., M.Eng., and Ph.D. degrees in electrical engineering from Cornell University, Ithaca, NY, USA, in 1984, 1985, and 1988, respectively.,He was on leave at the École Nationale Supérieure des Télécommunications, Paris, France, in Fall 1986. He was a Member of Technical Staff of AT&T Bell Laboratories from 1988 to 1991. Since 1991, he has been with The Chinese University of Hong Kong, where he is currently a Choh-Ming Li Professor of information engineering and the Co-Director of the Institute of Network Coding. He has held visiting positions at Cornell University, Nankai University, Bielefeld University, the University of Copenhagen, the Tokyo Institute of ... Show More

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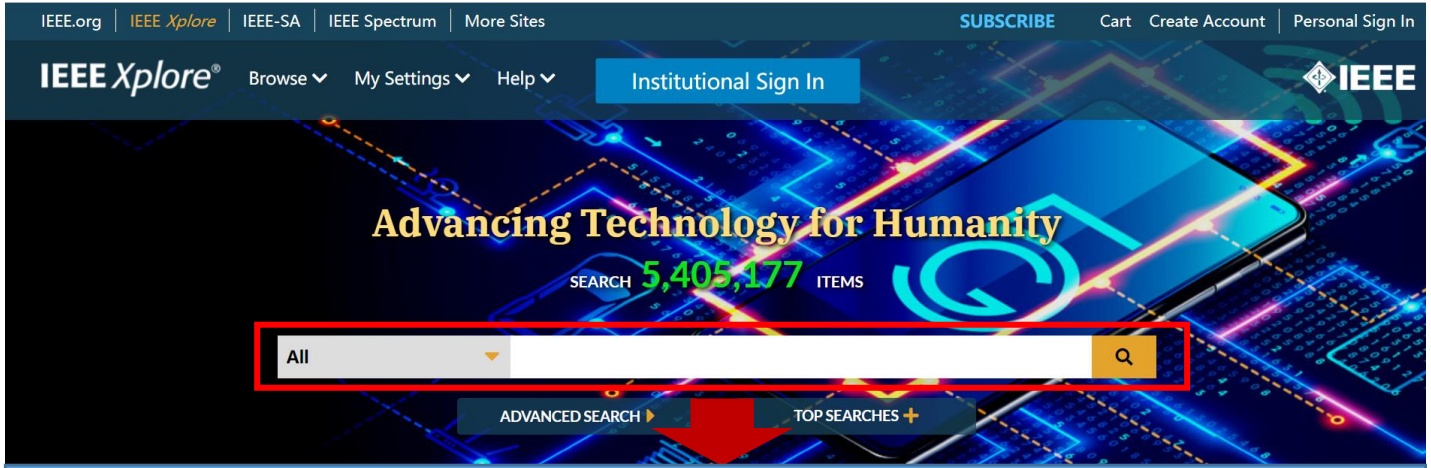

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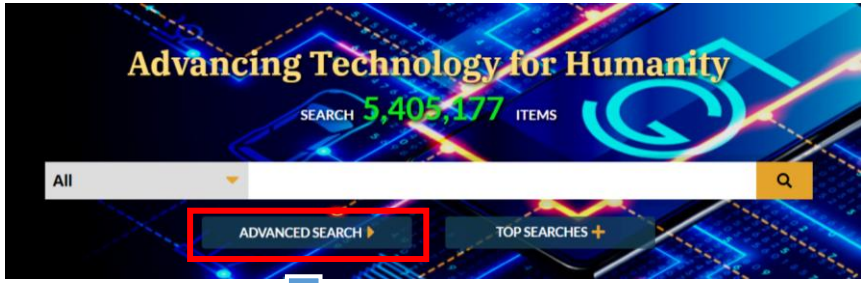

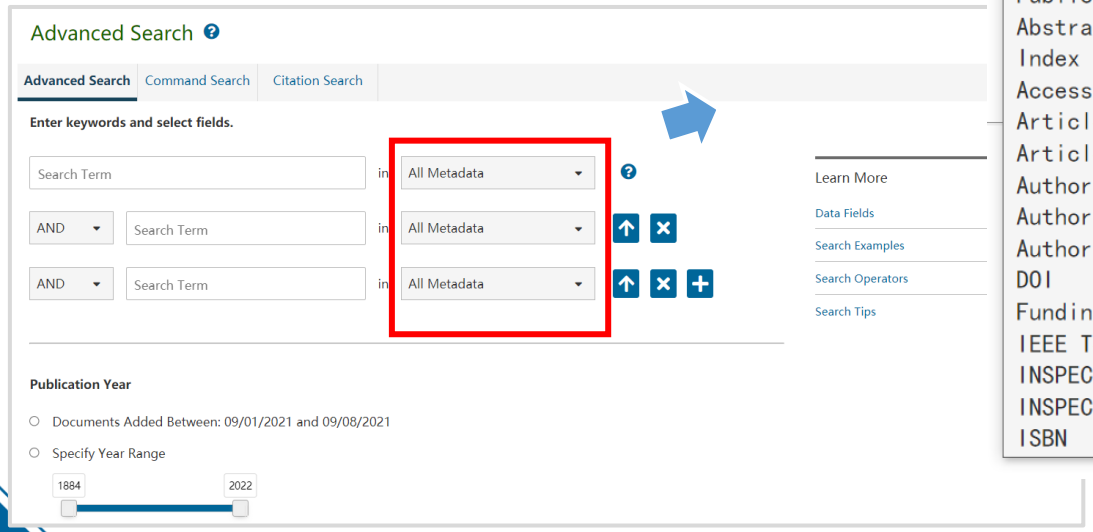

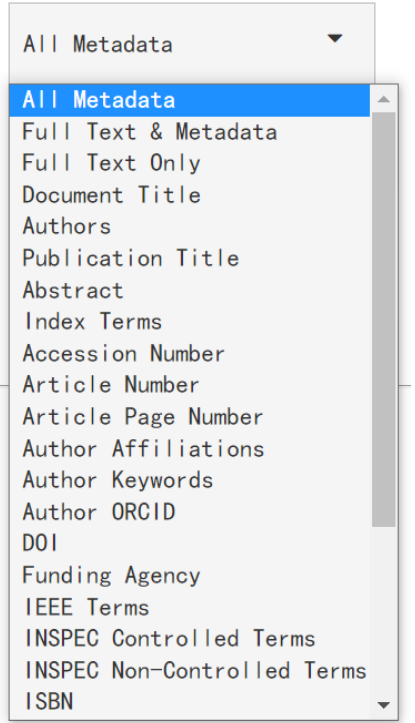

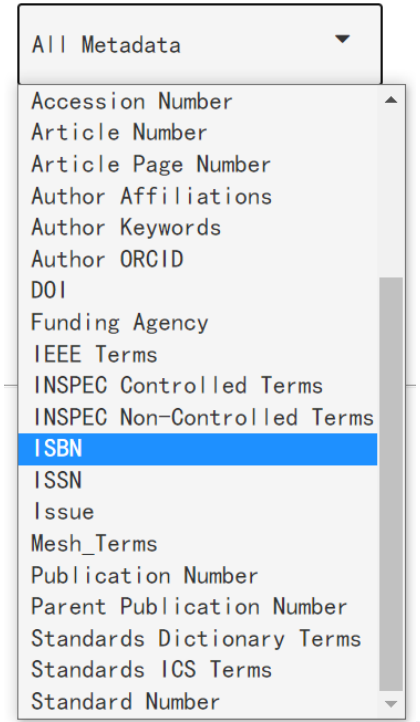

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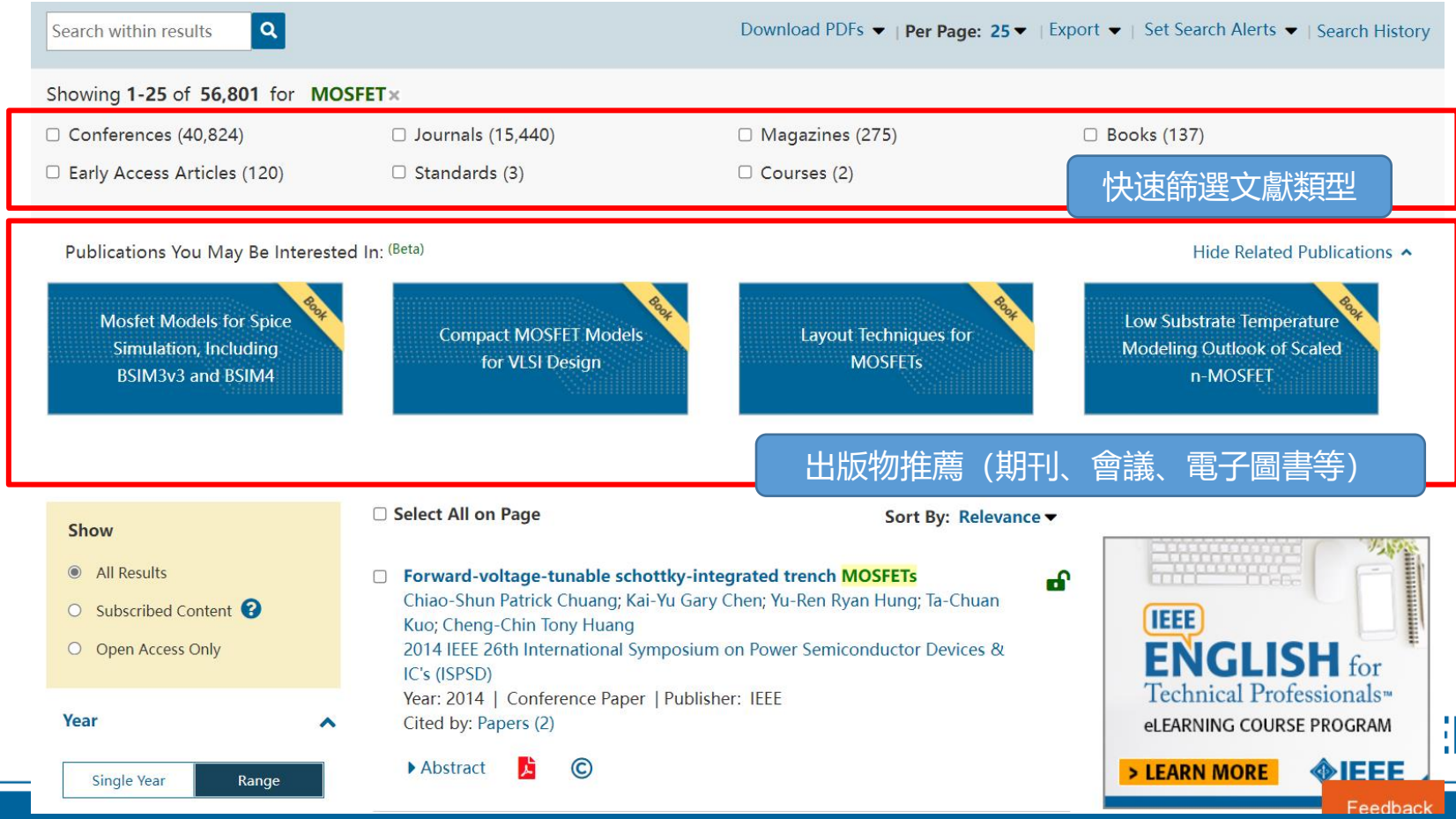

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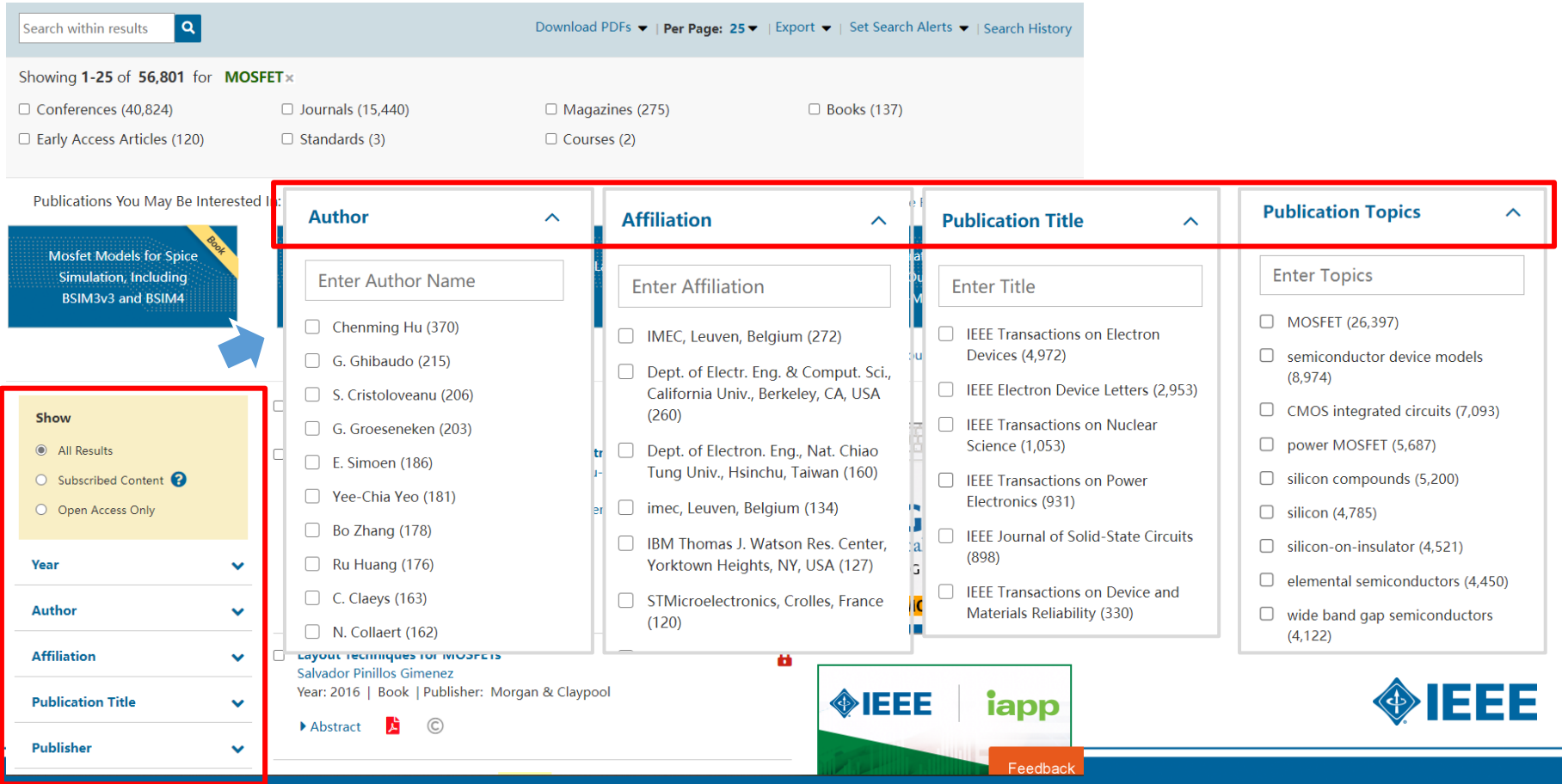

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Qi Wang; Ihsiu Ho; Minhua Li

IEEE Electron Device Let

Year: 2009 | Volume: 30, Issue: 1 | Journal Article | Publisher:

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☐ **Fabrication and Characterization of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET)-based Micro pH Sensor**

文章細節頁面

Hybrid MOSFET/driver for ultra-fast switching

T. Tang; C. Burkhart

IEEE Transactions on Dielectrics and Electrical Insulation

Year: 2009 | Volume: 16, Issue: 4 | Journal Article | Publisher: IEEE

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Abstract

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Abstract:

The ultra-fast switching of power MOSFETs, in about 1 ns, is very challen... the parasitic inductance that is intrinsic to commercial packages used fo... drivers. Parasitic gate and source inductance not only limit the voltage ri... internal gate structure but can also cause the gate voltage to oscillate. This paper describes a hybrid approach that substantially reduces the parasitic inductance between the driver and MOSFET gate, as well as between the MOSFET source and its external connection. A flip-chip assembly is used to directly attach a die-form power MOSFET and driver on a PCB. The parasitic inductances are significantly reduced by eliminating bond wires and minimizing lead length. The experimental results demonstrate ultra-fast switching of the power MOSFET with excellent control of the gate-source voltage.

推薦文獻

Published in: IEEE Transactions on Dielectrics and Electrical Insulation (Volume: 16 , Issue: 4, August 2009)

Page(s): 967 - 970 **INSPEC Accession Number:** 10847239

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SECTION I.
Introduction

Power MOSFETs have great potential as switches for high speed high voltage applications like pulsed power. the theoretical carrier transit time from drain to source is on the order of 200 ps in any cell of the silicon die [1]. Although the power MOSFET is

:/761685/

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IEEE Transactions on Power Electronics
Published: 1999

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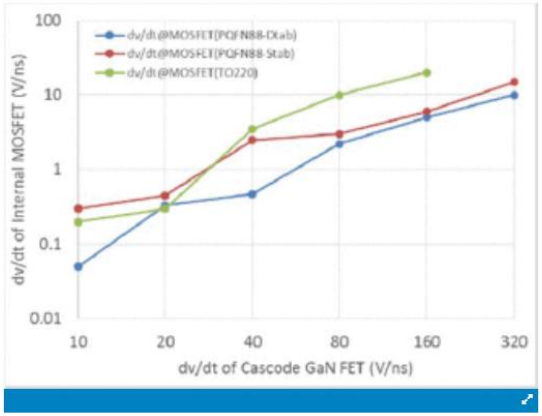

Dv/dt inside GaN FET in PQFN88 (drain tab) package and TO-220 package

Figure 10

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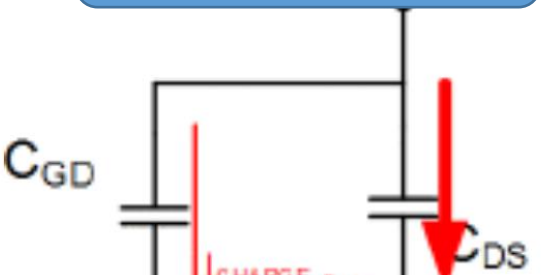

MOSFET is the most popular semiconductor switch and has been widely used in power electronics systems, like power supply, PFC, etc. Recently, it is also used in cascode GaN FET [1], as shown in Figure 1. In order to achieve high efficiency, MOSFETs nowadays are designed with very low parasitic capacitances and inductances. Combined with well-designed PCB layout, MOSFETs switches at nano-seconds [2] [3]. However, GaN HEMT

2. "Application Advantages and Disadvantages of Modern Fast Switching MOSFETs in VRM", *PCIM Europe*, 2016.

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1. Can MOS FET?

快速定位參考文獻

of the semiconductor was proposed in [23], and was defined as:

$$\sum_{SC} = \sum_{chip} + \sum_{pack,x} = \left(\sum_{n} \sigma_{chip,x(n)} A_{chip,n}\right) + \sum_{pack,x} \quad (1)$$

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\begin{align*}& \sum \nolimits _{\text {SC}} =\sum \nolimits _{\text {chip}}
+\sum \nolimits _{\text {pack,}x} \\& \qquad \qquad\qquad\qquad =\left ({{\sum
\limits _{n} {\sigma _{\text {chip,}x\left ({n}\right)} \,A_{\text {chip,}n}}}
}\right)+\sum \nolimits _{\text {pack,}x}\tag{1}\end{align*}
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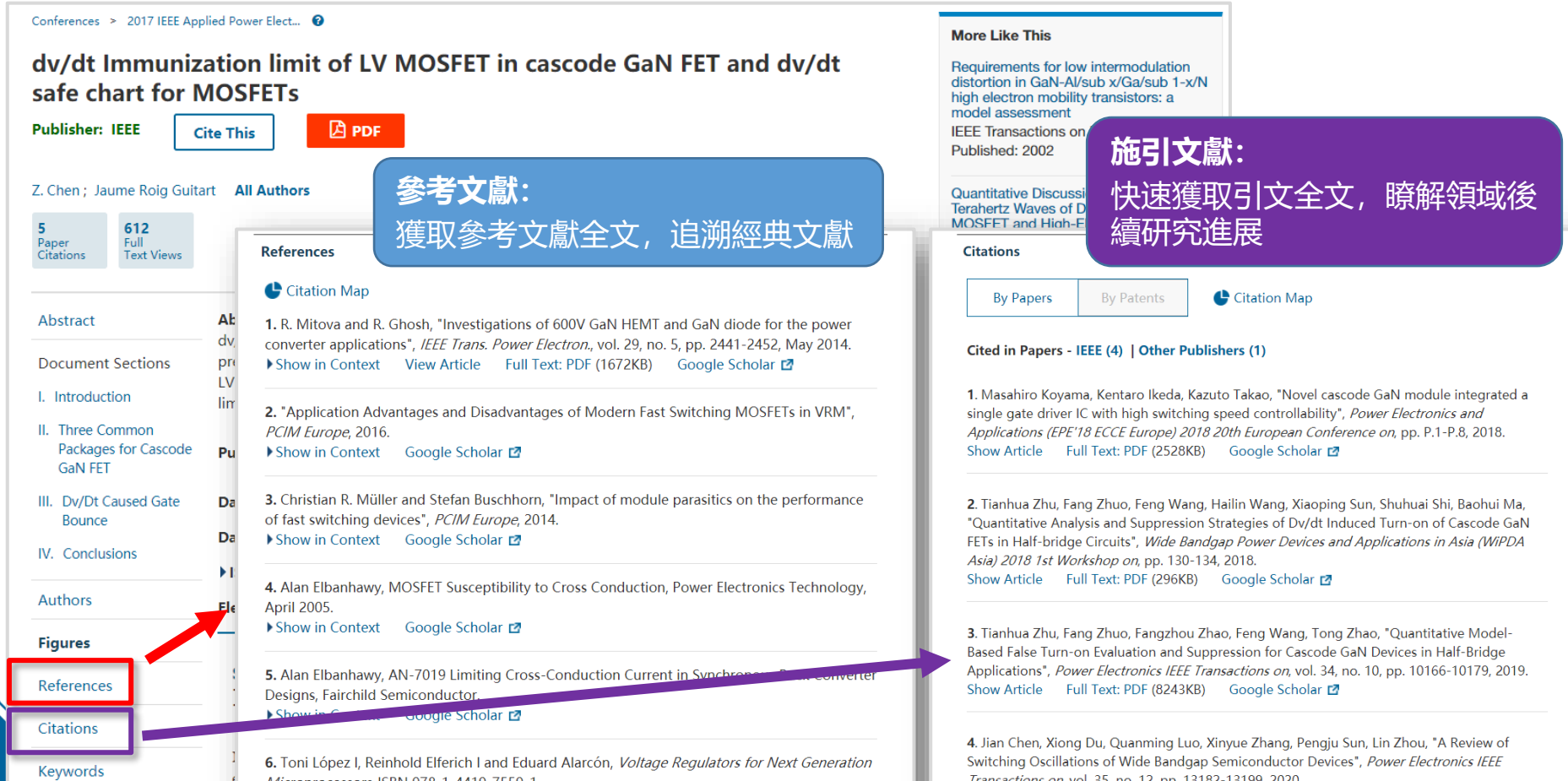

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Threshold voltage, MOSFET, Semiconductor device modeling, Electric potential, Semiconductor process modeling, Analytical models, Logic gates

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BSIM6 MOSFET model, physical charge-based core, short channel effects, SPICE simulators, IBM technology, threshold voltage extraction technique, size 90 nm

Author Keywords

BSIM6, MOSFET, SPICE

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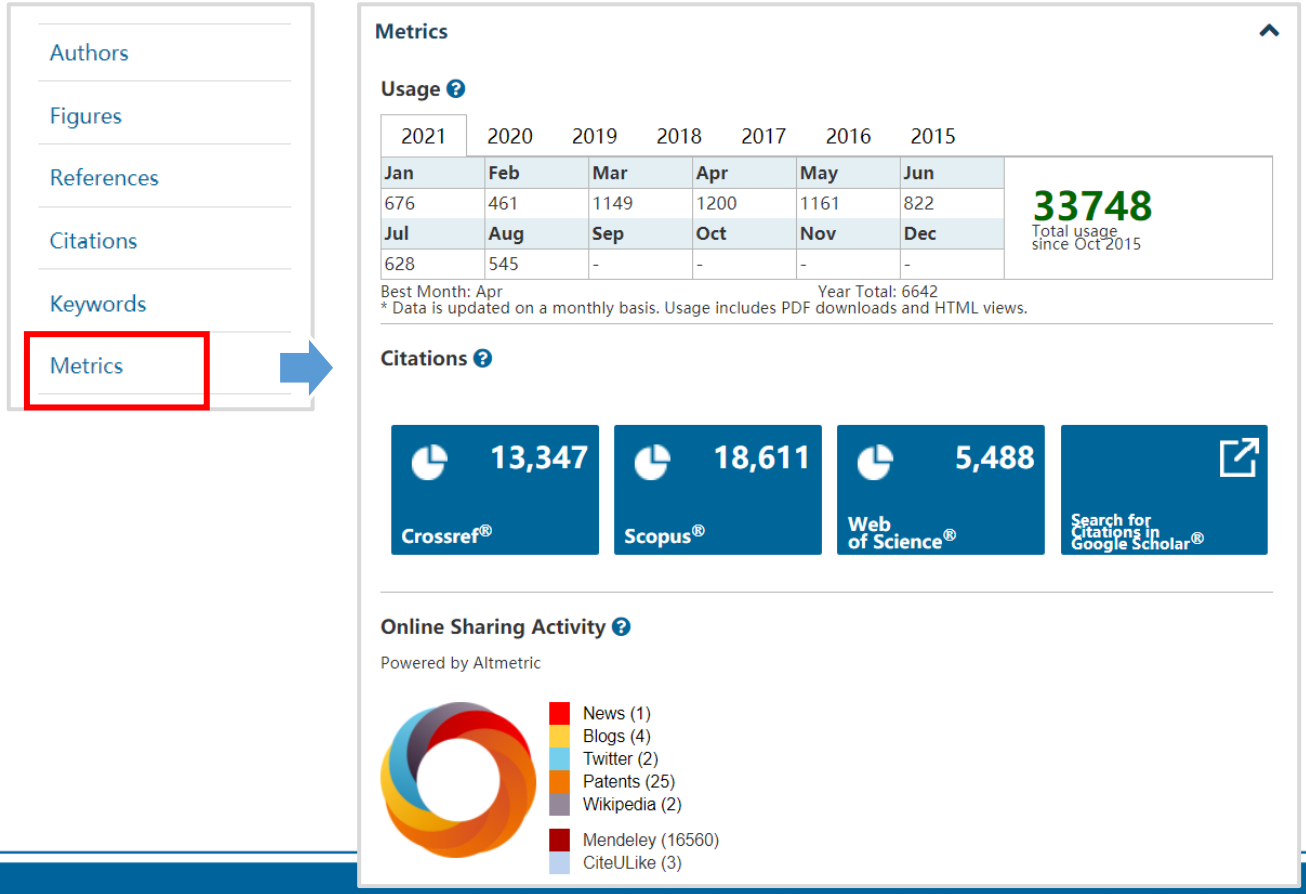
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628 545 - - - -
33748
Total usage since Oct 2015
Best Month: Apr
Year Total: 6642
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Analytical Modeling and Experimental Validation of Threshold Voltage in BSIM6 MOSFET Model

Publisher: IEEE | Cite This | PDF

Harshit Agarwal ; Chetan Gu

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Chenming Hu

Department of Electrical Engineering and Computer Science, University of California, Berkeley, Berkeley, CA, USA

瞭解作者詳情

Chenming Hu (F’ 03) is the TSMC Distinguished Professor Emeritus of University of California Berkeley, Berkeley, CA, USA. He is a Former Chief Technology Officer of TSMC. He is a Board Director of SanDisk Inc., and of the non-profit Friends of Children with Special Needs. He is well known for his work on the 3-D transistor, FinFET, which can be scaled to single digit nanometers. He has developed widely used IC reliability models and led the research of BSIM—the first industry—standard SPICE model used by most IC companies to design CMOS products since 1996. He was a recipient of the IEEE Andrew Grove Award, the Solid State Circuits Award and Nishizawa Medal, the Kaufman Award of the EDA industry, the University Research Award of the U.S. Semiconductor Industry Association, and the UC Berkeley’ s Highest Honor for teaching—the Berkeley Distinguished Teaching Award.

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IEEE Transactions on Electron Devices
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Chenming Hu

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Department of Electrical Engineering and Computer Science
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Publication Topics
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Biography
Chenming Hu (LF' 03) is currently a Distinguished Professor Emeritus with the University of California at Berkeley, Berkeley, CA, USA. He is also the Board Director of SanDisk Inc., San Jose, CA, USA, and Friends of Children with Special Needs, Fremont, CA, USA. He is known for his involvement in FinFET–the 3-D transistor, widely used IC reliability models, and BSIM–the industry standard transistor models used by most IC companies since 1997 to design CMOS products. *(Based on document published on 29 August 2018).*

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Guohua Wu; Xupeng Wen; Ling Wang; Witold Pedrycz; P. N. Suganthan

IEEE Transactions on Evolutionary Computation

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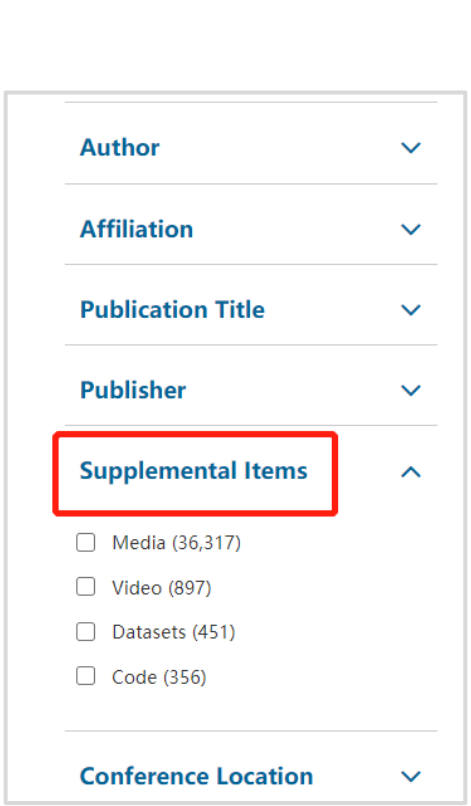

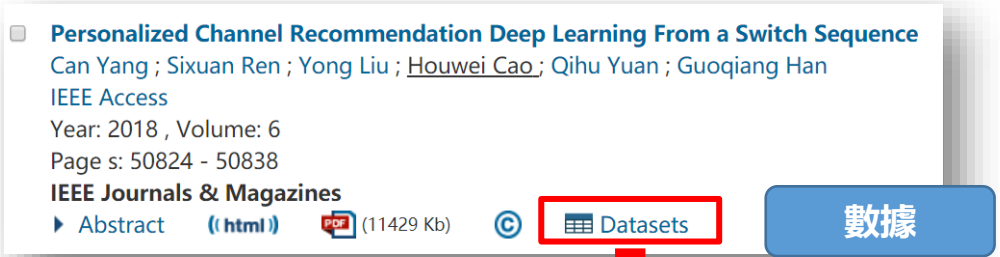

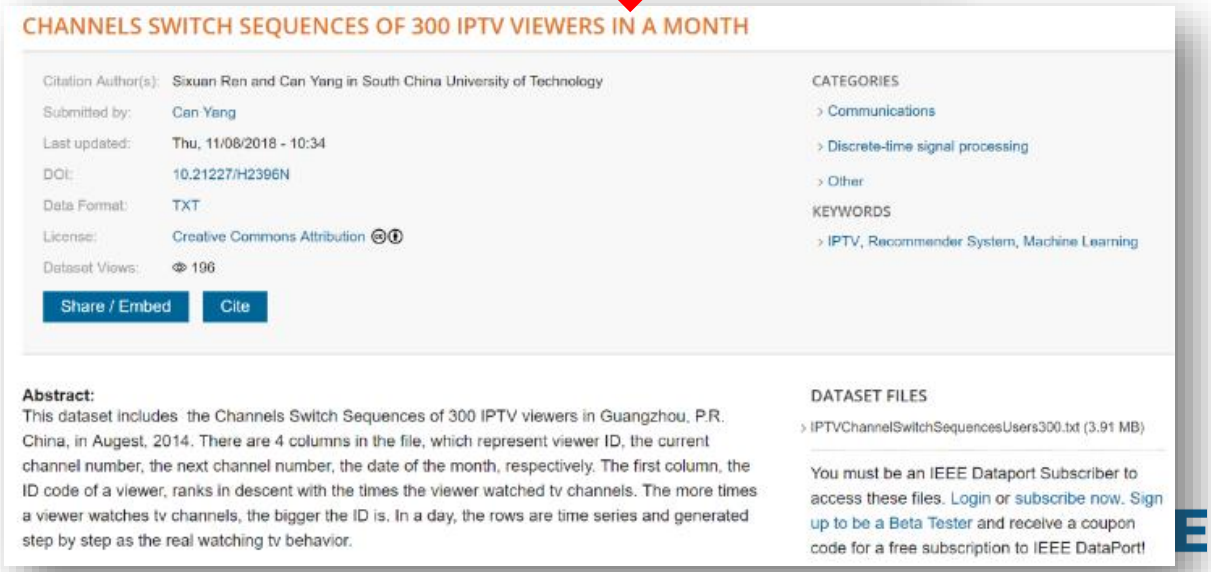

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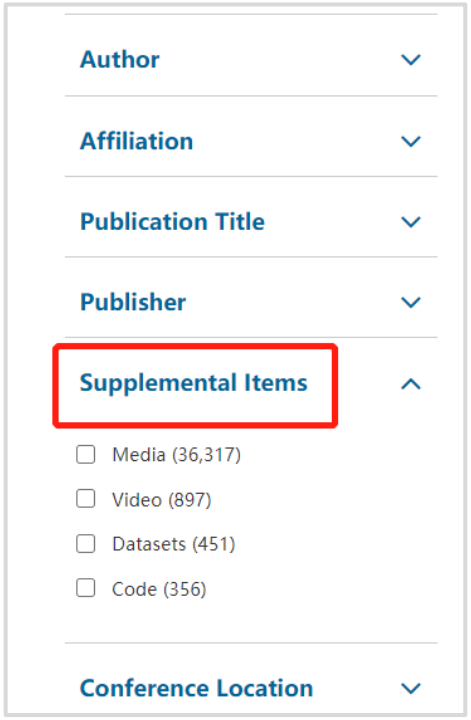

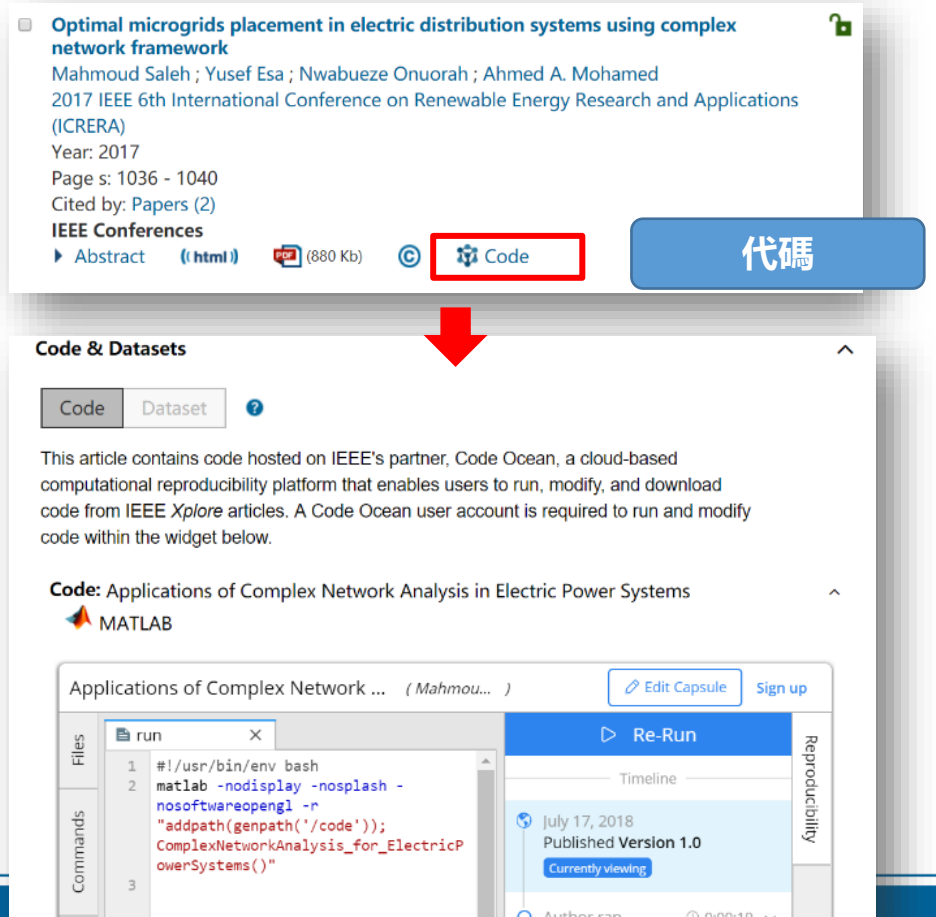

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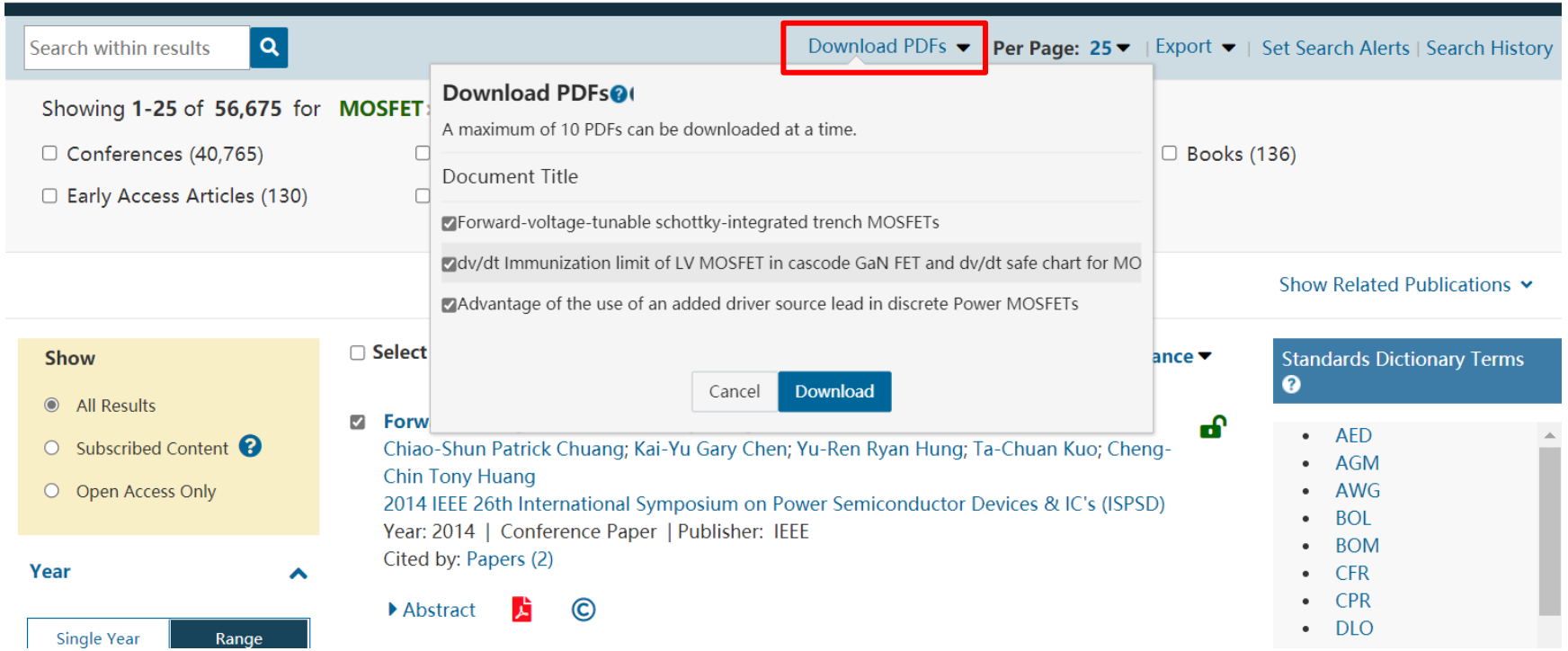
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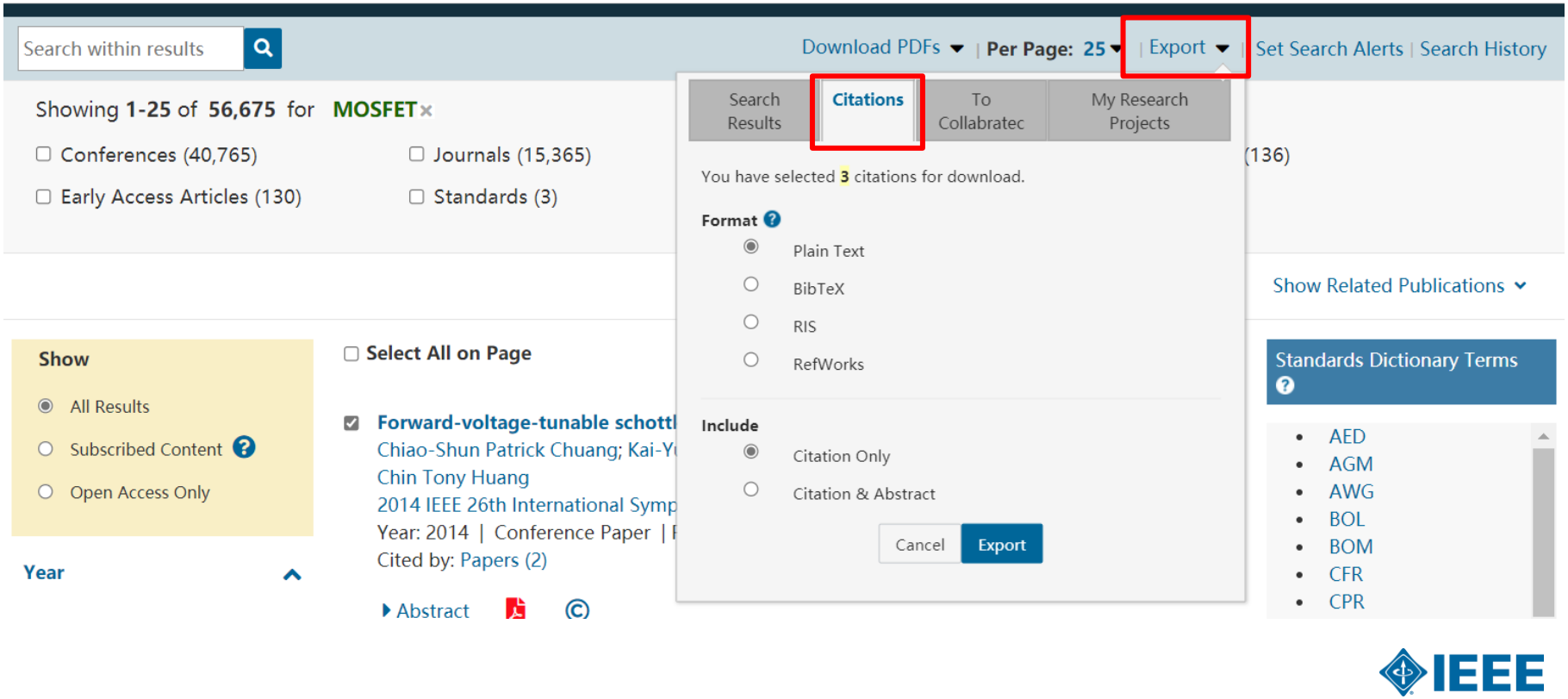
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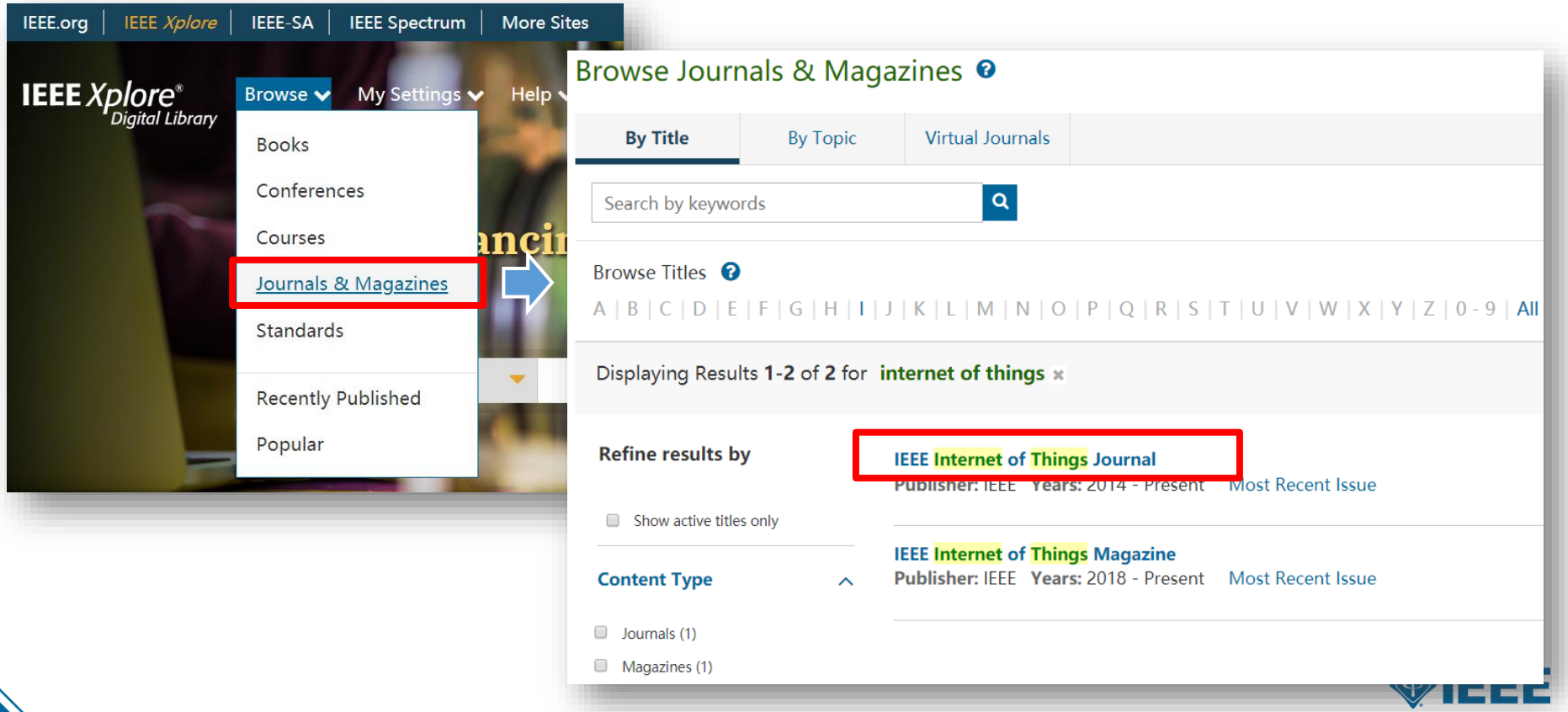
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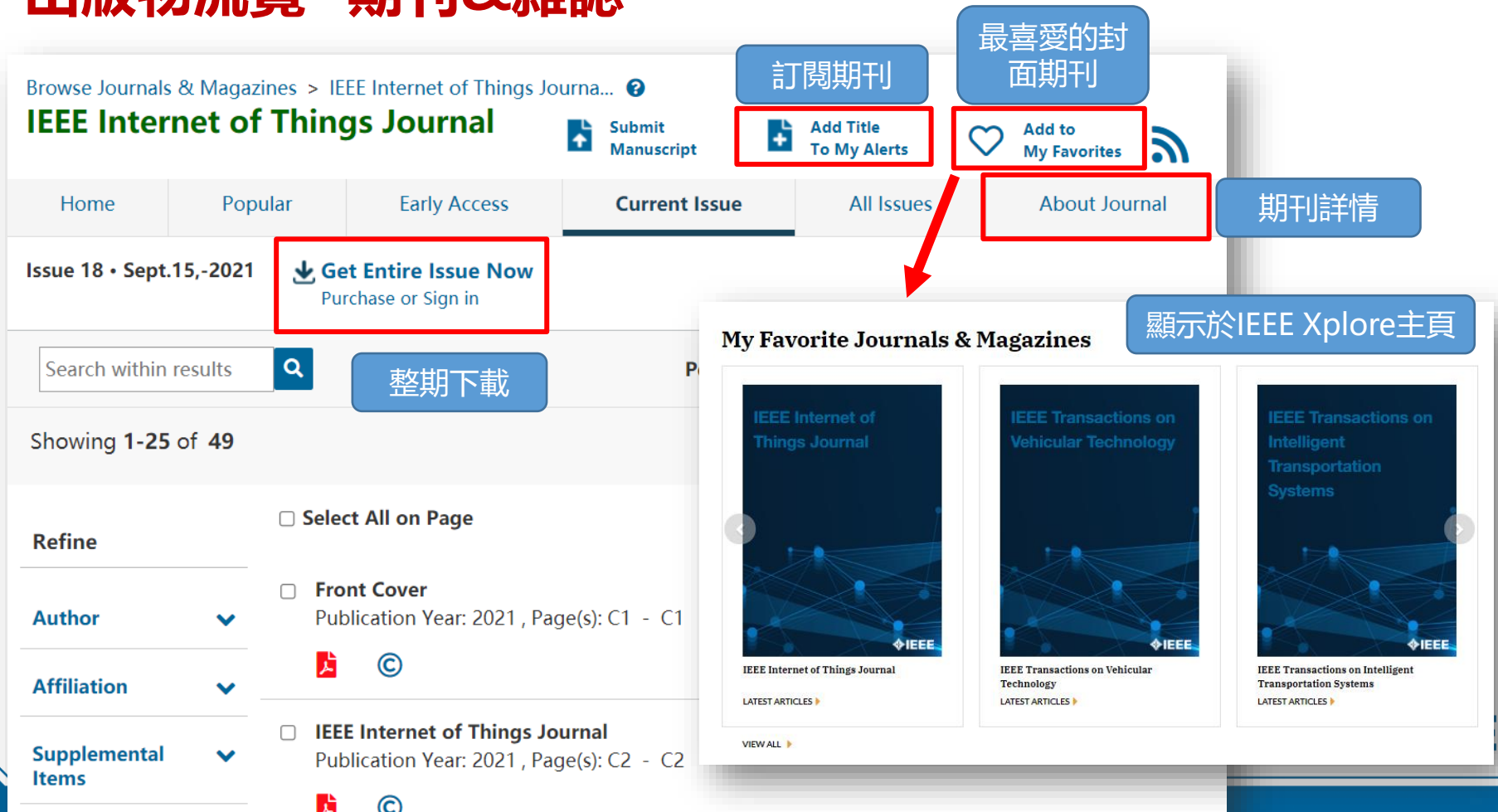
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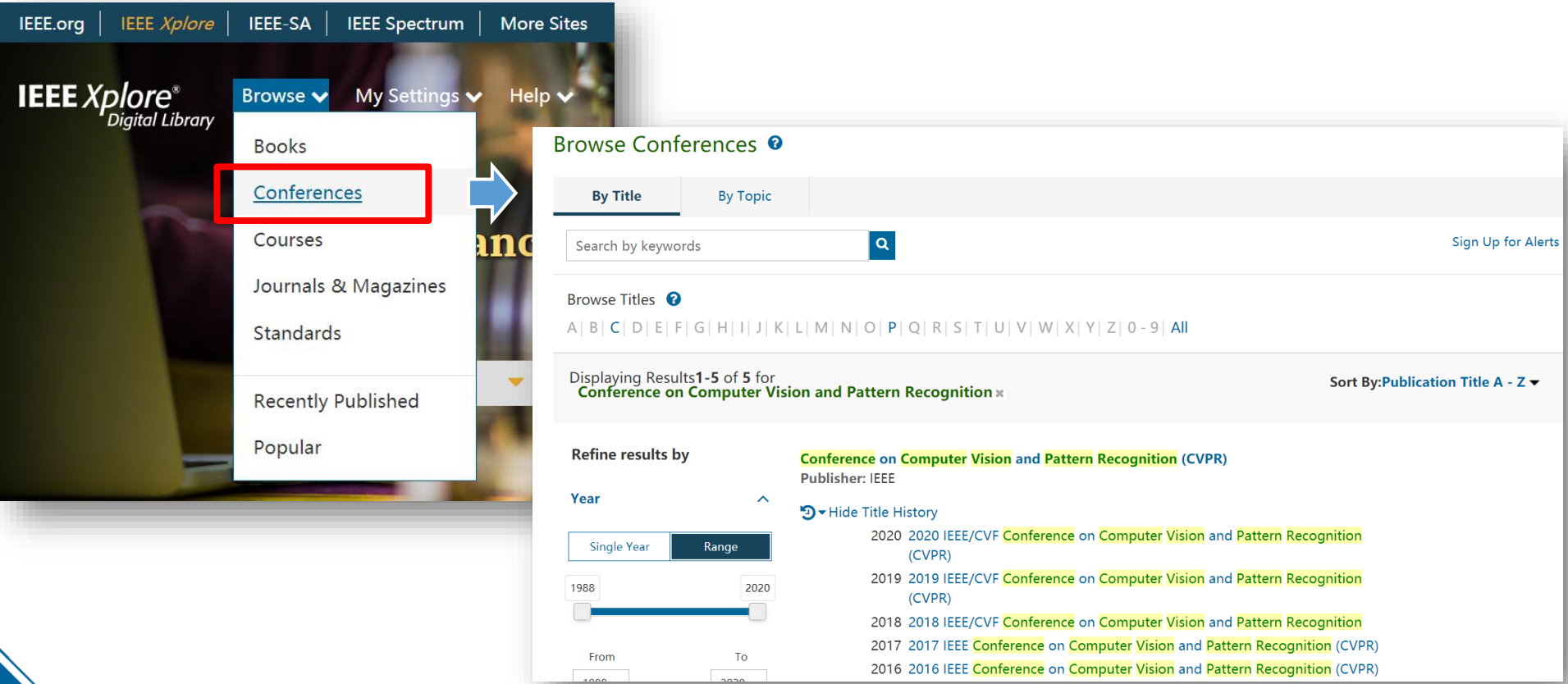
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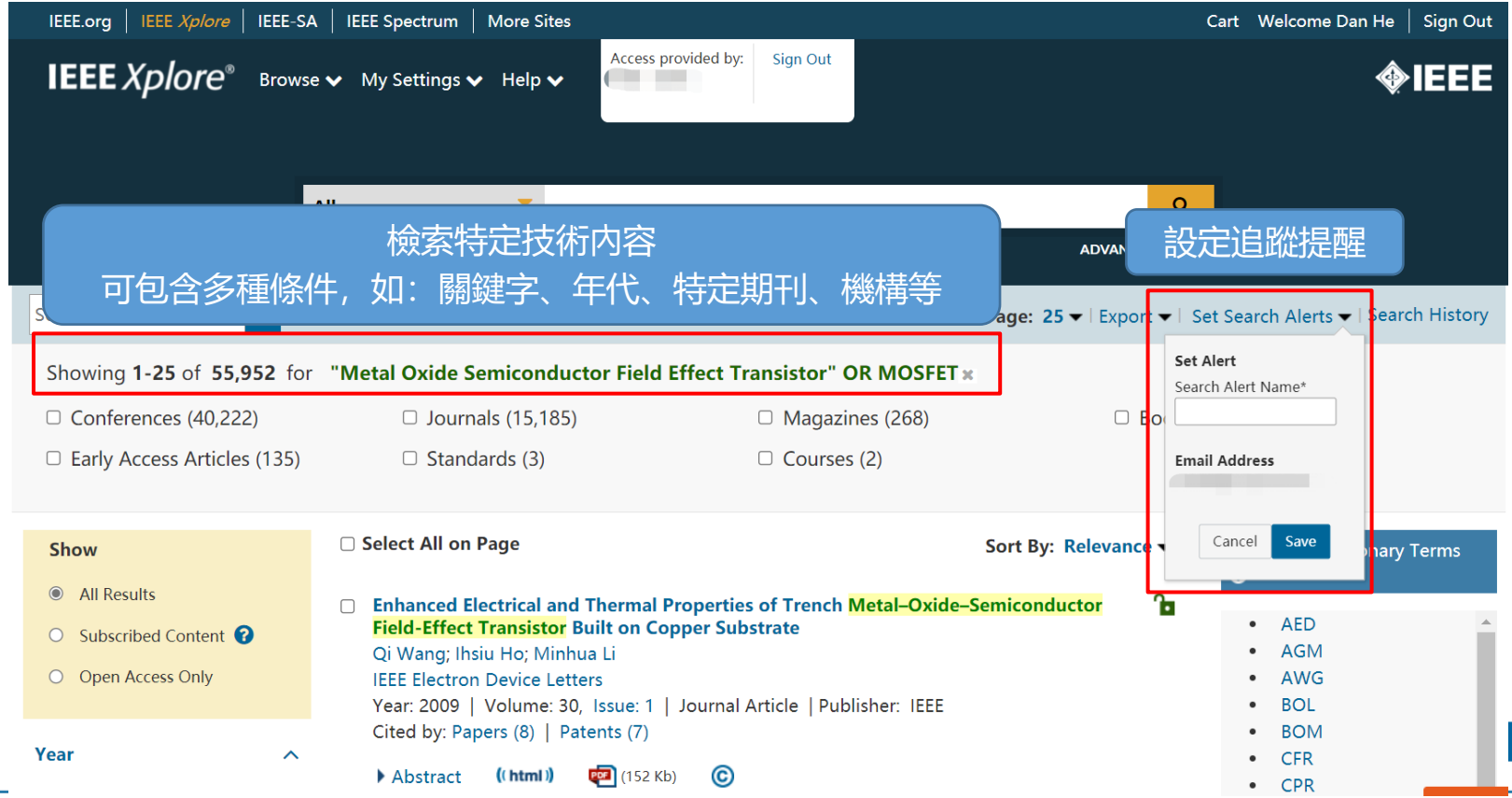

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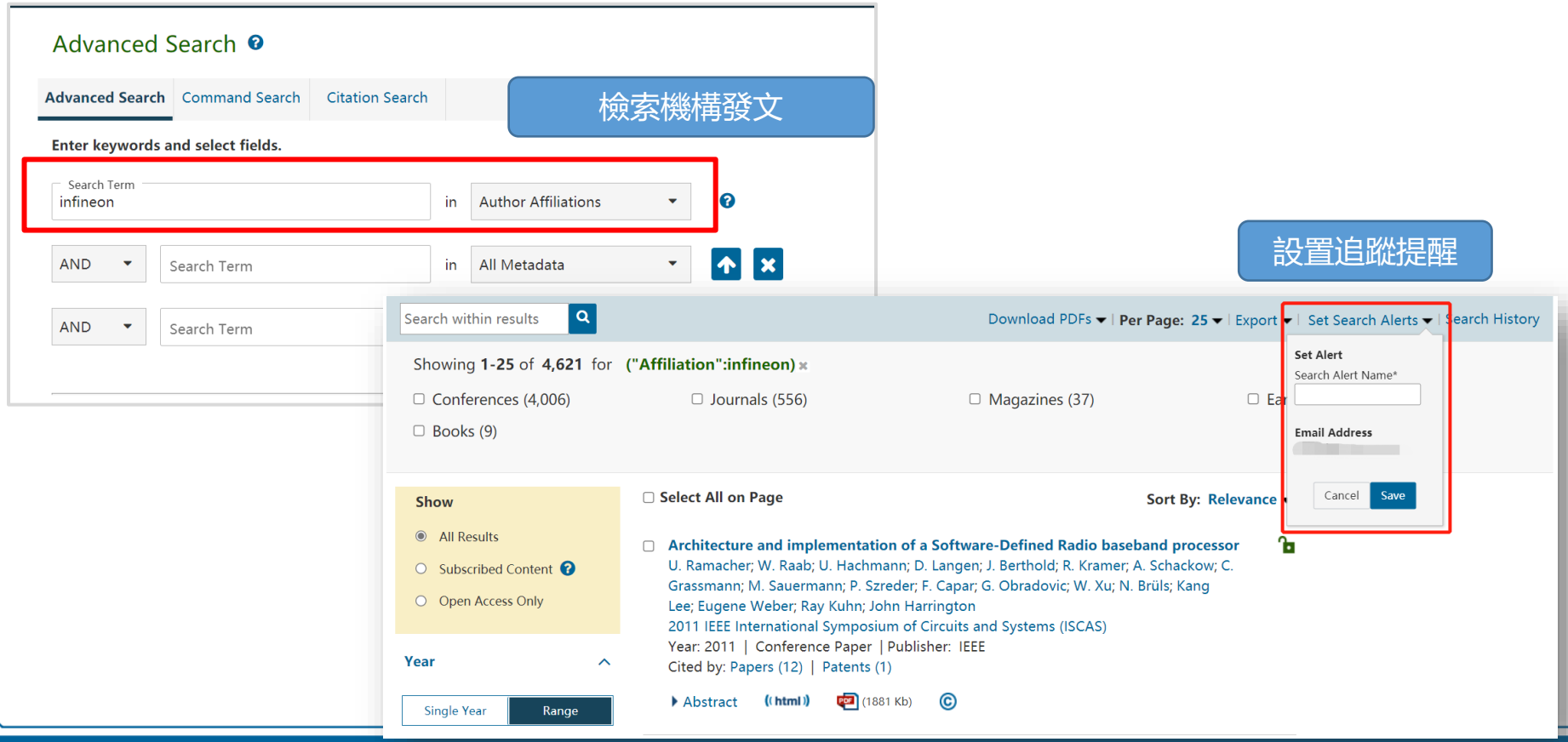

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Biography
Hans Reisinger received the Diploma degree in physics and the Ph.D. from the Technical
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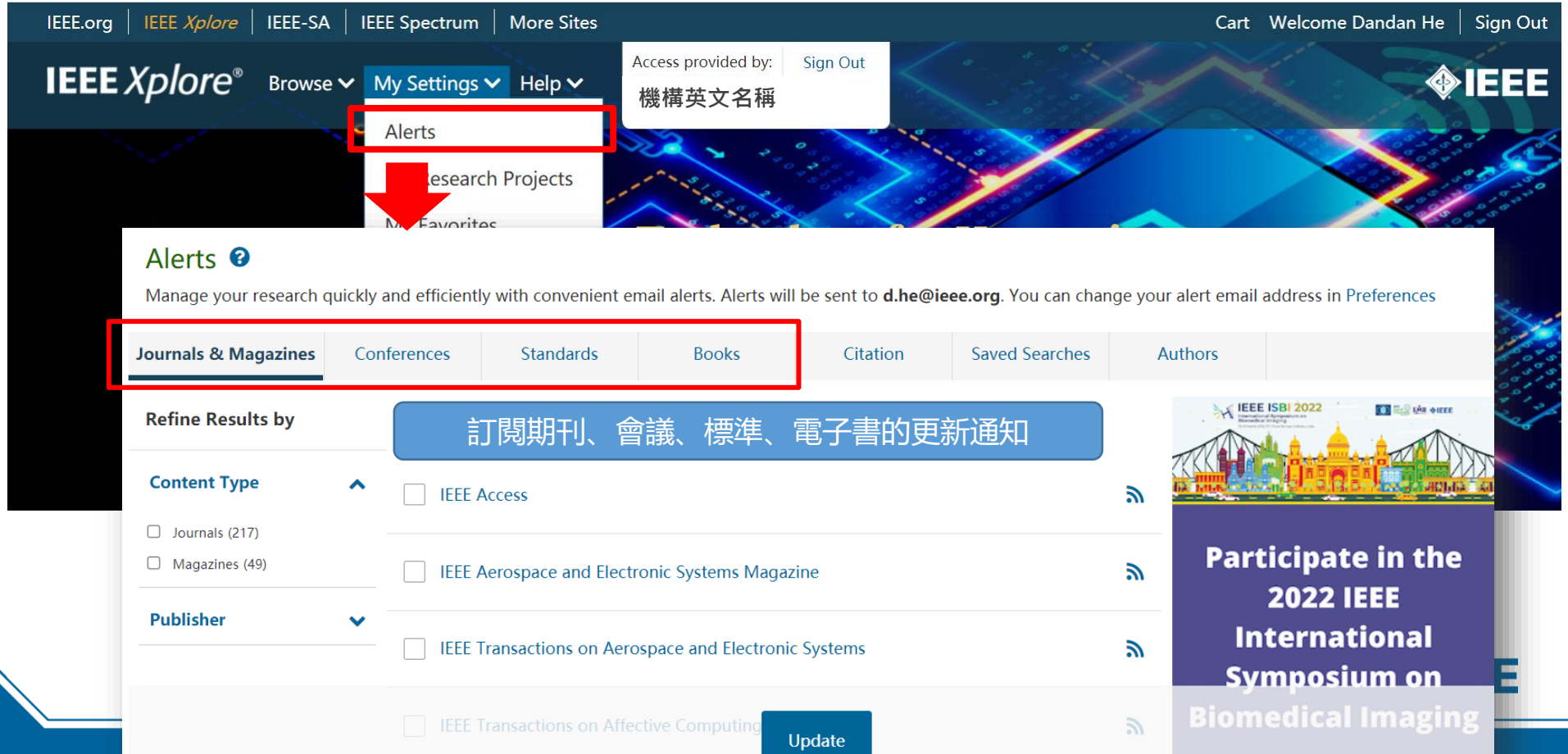

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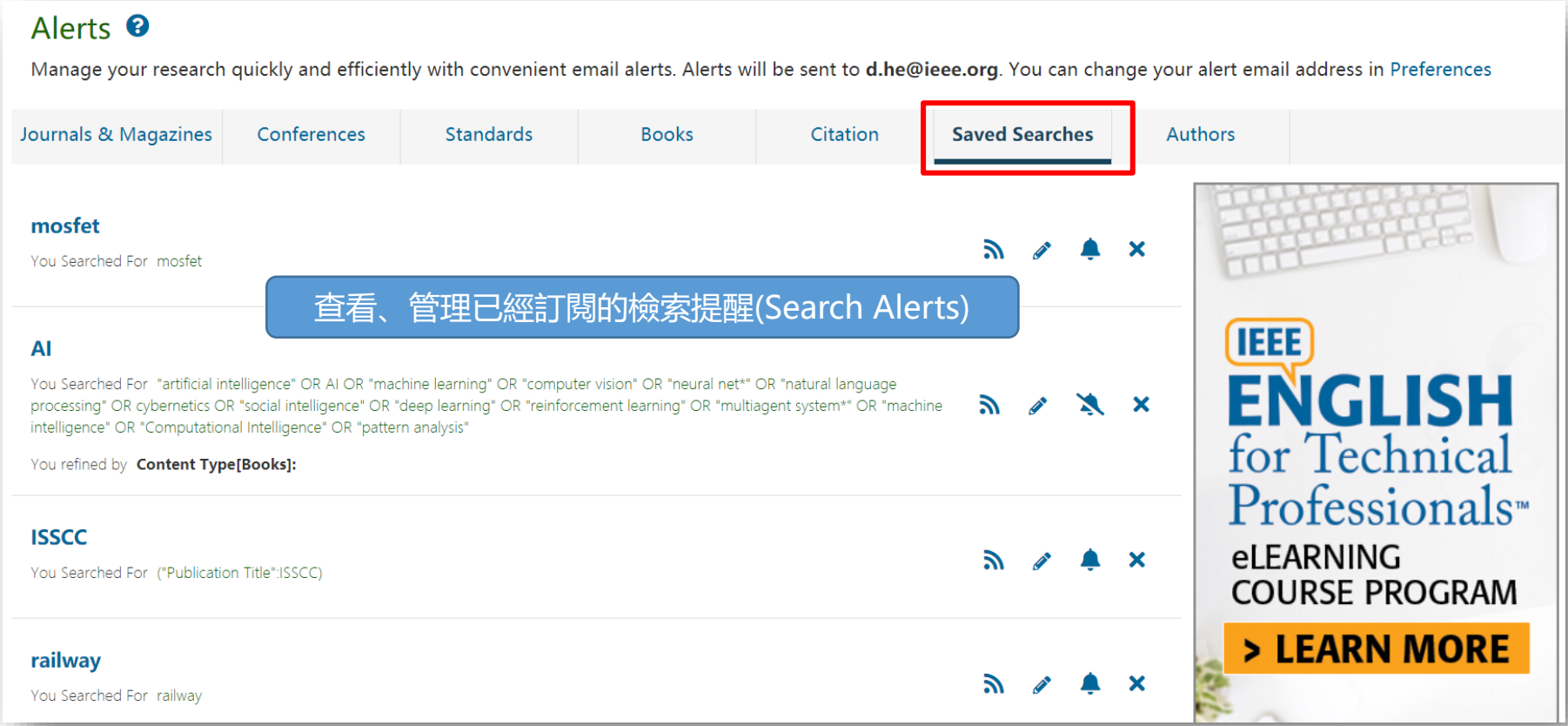

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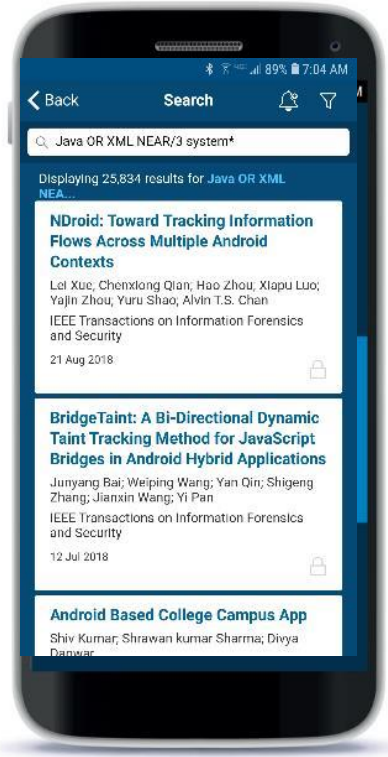

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